Homework 9
Due Wednesday, November 16

INTERRUPTS

Read Chapter 7.7, 8.6
Do Chapter 7 # 8, 9

1. True/False
    a.   Interrupts are asynchronous
    b.   ISRs always run in supervisor state.
    c.   Your code can initiate an interrupt with a TRAP instruction.
    d.   An ISR should terminate with an RTE.
    e.   All interrupts can be masked (prevented) by the I0 - I2 bits of the SR.

2. What is polling? Why is interrupt driven I/O better than polling?

3. Suppose you have a device which detects cars. Every time a car runs over the
    device, the device generates a level 2 interrupt. You install the following ISR:

    ```
    ISR           MOVE          COUNT,D0
                  ADD           #1,D0
                  MOVE          D0,COUNT
                  RTE
    ```

    This code messes up D0. Why is this a serious problem? How could you fix it
    (hint: use the stack).

4. Memory contains:
    ...
    $000060:   0000 0000 0000 8000 0000 8006 0000 800C
    $000070:   0000 8010 0000 8016 0000 0000 0000 0A16
    ....
    Assume you're using autovectored interrupts.
    a)   At what address does the ISR for a level 3 interrupt begin?
    b)   At what address does the ISR for the level 7 interrupt begin?