Homework 11
Due Wednesday, December 7

INTEL 8086

1. Explain the difference between little-endian and big-endian storage of words.

2. The 68000 has separate data and address buses. The 8086 has a multiplexed data and address bus. What's an advantage of each over the other?

3. What is the Parity Flag on the 8086?

4. The 16-bit AX register on the 8086 can be used as two single byte registers AH and AL. What's the difference between this and the .B, .W on the 68000.

5. With a 20 bit address bus, how much memory can the 8086 access?

6. How does the 8086 get 20 bits of address space while only storing 16 bit addresses in memory?

7. Give some pros and cons of memory-mapped versus isolated I/O.

RISC

8. What is an instruction pipeline?

9. The MIPS RISC processor breaks each instruction into five stages, with each stage taking one machine cycle. How many instructions per cycle could the MIPS (potentially) average?

10. The JSR/BSR instructions of the 68000 need to push a return address onto the stack. In a pipelined machine, this push takes extra steps that would stall the pipeline. RISC machines get around the problem by not pushing the address at all. Instead, a jump to subroutine stores the return address in one of the registers. This could cause problems for subroutines that call other subroutines. Why?

    To get around this, software needs to push the return address using a separate store instruction.